US PAT NO: 5686747

DOCUMENT IDENTIFIER: US 5686747 A
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TITLE: Integrated circuits comprising interconnecting plugs

KWIC

Detailed Description Text DETX 13 :
patterning a bit **contact opening through the bit line** insulating layer to outwardly expose electrically conductive first layer material within the second contact openings; and

Detailed Description Text DETX 33 :
Referring to FIG. 3, a first layer 36 of electrically conductive material is provided over insulating material layer 28 to within first contact opening 32 and second contact opening 34 to electrically connect with first and second active regions 26 and 24, respectively. First layer 36 is deposited to a thickness which less than completely fills first contact opening 32 and second contact opening 34, thereby leaving outwardly open first voids 35 within the first and second contact openings. An example diameter for first **contact opening 32 are 0.6 micron, while example dimensions for second contact opening** 34 are 0.6 .times.1.0 micron. In such instance, an example preferred thickness for layer 36 is 1000 Angstroms. An example and preferred material for layer 36 is hemispherical grain HSG polysilicon. Such can be provided by first depositing a 600 Angstroms thick in situ doped polysilicon layer, followed by

deposition of undoped HSG poly. Subsequent heating inherent in wafer processing will effectively conductively dope the overlying HSG poly layer. Alternately, layer 36 can be provided by in situ arsenic doping of an entire HSG layer.

Detailed Description Text DETX 38 :

Referring to FIG. 8, a bit line insulating layer 44 (e.g., BPSG) is provided outwardly of second electrically conductive material layer 40 and to within third voids 39. A bit **contact opening 45 is patterned through bit line** insulating layer 40 to again outwardly expose electrically conductive first layer material 36 within second contact opening 34.

Detailed Description Text DETX 40 :

The above described process etches capacitor dielectric layer 38 and second conductive layer 40 away from over second **contact opening 34 prior to provision of bit line** insulating layer 44. An alternate process wherein such etching is conducted after provision of bit line insulating layer 44 is described with reference to FIGS. 10-14. FIG. 10 illustrates the FIG. 6 wafer at a processing step immediately subsequent to FIG. 6 which differs from that shown in FIG. 7. Like numbers are utilized from the first described embodiment where appropriate, with significant differences being indicated by addition of a suffix "a" to the FIGS. 10-14 embodiment. FIG. 10 shows fragment 10a having bit line insulating layer 44a deposited atop previously un-patterned layers 40 and 38.

Detailed Description Text DETX 42 :

The FIGS. 10-14 process in comparison with the first described embodiment,

while having the advantage of reduced masking steps, does have the disadvantage
of providing greater parasitic capacitance between the bit **line plugging material within contact opening** 43 the result of closer proximity of such
material to second cell poly layer 40 than in the first described embodiment.

US PAT NO: 5847461

DOCUMENT IDENTIFIER: US 5847461 A

TITLE: Integrated circuit structure having contact openings and vias filled by self-extrusion of overlying metal layer

KWIC

Brief Summary Text BSTX 7 :

Aluminum has been the metal or alloy of choice for use in the formation of patterned interconnects or "wiring" on the surface of insulating layers, due to its high conductivity, low cost, and compatibility with other materials used in the construction of the integrated circuit structure. In the past, when larger **dimensions were used for line widths and contact opening** diameters, contact openings or vias were formed in the insulating layer and a layer of aluminum was then formed over the insulating layer which also filled the contact openings as well, although barrier material, such as TiN was usually used when the aluminum would otherwise contact silicon, to avoid migration of Si or Al atoms into the other material.

Brief Summary Text BSTX 8 :

However, as **dimensions of lines and contact openings** decreased, with ever increasing scale of VLSI structures, problems arose with securing satisfactory filling of the entire contact opening with the aluminum used to form the contact layer over the insulating layer. This, in turn, has given rise to the use of other filler materials such as tungsten to fill the

contact opening
prior to the formation of the aluminum layer over the insulating layer. After
formation of, for example, a barrier layer of TiN, a layer of tungsten is
deposited over the barrier layer and insulating layer which also fills the
contact opening after which the structure is planarized to remove all of the
surface tungsten leaving only the tungsten in the contact openings . The
aluminum layer is then formed over the insulating layer which aluminum layer
thereby makes electrical contact with the upper exposed surface of the
underlying tungsten in the contact opening.

US PAT NO: 5994237

DOCUMENT IDENTIFIER: US 5994237 A

TITLE: Semiconductor processing methods of forming a contact opening to a semiconductor substrate

KWIC

Brief Summary Text BSTX 7 :
Referring to FIG. 2, one prior art problem associated with forming a contact opening to wafer or substrate 10 is illustrated. Typically, a **contact opening 28 is anisotropically etched between conductive lines** 14 to a degree sufficient to expose an area 30 of the substrate between the conductive lines and to which electrical connection is to be made.

Brief Summary Text BSTX 9 :
Referring to FIG. 3, a prior art solution to the above described problem is shown in which **contact opening 28 is made to be narrower between conductive lines** 14. As shown, the sides of contact opening 28 coincide with inner most side wall spacers 22 so that the risk of overetching the side wall spacers and hence nitride caps 20 and silicide 18 is reduced. However, such trade offs in contact opening width and the reduced risk of overetch place sever constraints on the photomask alignment processes used to define contact opening 28.

Detailed Description Text DETX 5 :
Referring to FIG. 5, BPSG layer 52 is patterned and etched over contact area 48 to form a **contact opening 54 between conductive lines**

38. Preferably, such etch is an anisotropic dry etch which is conducted through layer 52 to a degree sufficient to leave at least a portion 56 of TEOS layer 50 over contact area 48 at the bottom of the contact opening. Exemplary conditions for such an etch in an Applied Materials 5000 reactor are 45 mTorr, 900 W, 40 Gauss, 20 sccm CF.sub.4, 45 sccm CHF.sub.3, 80 sccm Ar, 9000 mTorr He backside pressure. Such etch might also be conducted as a second part of a 2 step etch, where the first etches oxide at a faster rate. Exemplary conditions in such instance for the first etch in the same reactor are 120 mTorr, 900 W, 90 Gauss, 20 sccm CF.sub.4, 50 sccm CHF.sub.3, 110 sccm Ar, 28 sccm N.sub.2, 9000 mTorr He backside pressure. For purposes of the ongoing discussion, that portion of layer 52 which is etched and that portion of layer 50 which is left behind constitutes material between conductive lines 38 which is etched to a degree sufficient to leave at least some of the material (i.e., portion 56) over the substrate between the conductive lines. Such etch defines a contact opening 54 having a first lateral width dimension W.sub.1. One advantage of leaving portion 56 behind over contact area 48 is that inner-most sidewall spacers 46 are not undesirably etched or overetched which prevents the above described shorting conditions (FIG. 2) which can render a device useless.

Detailed Description Text (DETX 6):

Referring to FIG. 6, at least some of substrate 34 between conductive lines 38, and preferably all of the substrate defining contact area 48, is outwardly exposed by a wet etch of portion 56 (FIG. 5). Such etch can be conducted using a suitable aqueous solution comprising fluorine atoms, such as an aqueous 0.5-

by weight HF solution, and NH.sub.4 F solution or a mixture thereof. Such solutions have a greater etch rate for BPSG layer 52 than for first oxide layer 50. A typical etch rate ratio for such a solution as between BPSG layer 52 and first oxide layer 50 is about 3:1. Accordingly, etch timing is controlled to avoid overetching BPSG layer 52 and the nitride encapsulated conductive lines. Preferably, however, such etch is conducted using an aqueous solution which has a greater etch rate for portion 56 and hence first oxide layer 50 than for BPSG layer 52. Such comprises a second etch which also preferably removes a desired amount of layers 50. 52 laterally outwardly of and beyond contact area 48 in a controlled manner to effectively increase the lateral width **dimension of the upper portion of contact opening** 54 to W.sub.2 as shown. Such increase in lateral width dimension is desirable from the standpoint of subsequent contact formation which utilizes a conductive material, such as conductively doped polysilicon which is deposited into contact opening 54 and forms a contact plug.

US PAT NO: 6165910

DOCUMENT IDENTIFIER: US 6165910 A

TITLE: Self aligned contacts for semiconductor device

KWIC

Brief Summary Text BSTX 7 :

The use of self aligned contacts advantageously permits circuit designers greater flexibility in the placement of the contact openings. In some instances, the use of self aligned contacts permits circuit designers to pack the gates more closely together since the minimal distance between the gates is not bounded by the **dimension of the contact opening** which is limited by, for example, the accuracy of the photolithography and the oxide etch processes.

Detailed Description Text DETX 5 :

In accordance with another embodiment of the present invention, the self aligned contact openings having an aspect ratio of equal to or greater than about 3:1 or a depth greater than about 0.75 micrometer are etched with a two-step etch process, which employs CHF.sub.3, C.sub.2 HF.sub.5, CH.sub.2 F.sub.2 and optionally argon, CF.sub.4 and/or C.sub.2 F.sub.6 as etchant source gases in a plasma processing chamber. In the first etch step, the contact opening is preferably etched with a first chemistry that includes CHF.sub.3 and C.sub.2 HF.sub.5 and first set of process parameters that are designed to, among others, prevent the occurrence of a spiked etch. Furthermore, the first

chemistry may preferably include argon, which further facilitates the prevention of a spiked etch and enhances photoresist selectivity. Further still, the first chemistry may also include CF.sub.4 and/or C.sub.2 F.sub.6 as etchant source gases in a plasma processing chamber. As the term is employed herein, a spiked etch represents a distortion in the etch sidewall such that the contact opening becomes progressively narrower at the bottom of the etch. As illustrated in FIG. 2, contact opening 44 is then to have a spiked etch when its sidewalls taper toward the **contact opening center line** 60 starting from a threshold position 62. In some cases, the critical **dimension of the contact opening** may narrow before the **contact opening sidewalls begin to taper toward center line** 60.

US PAT NO: 6319813

DOCUMENT IDENTIFIER: US 6319813 B1
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TITLE: Semiconductor processing methods of forming integrated circuitry and integrated circuitry constructions

KWIC

Detailed Description Text DETX 10 :
Referring to FIG. 5, a, portion of the insulative cap over the leftmost conductive line 16 has been removed to facilitate electrical connection therewith. A patterned masking layer 44 is formed over the plurality of layers 30 and defines a trench pattern, trough pattern, or conductive line pattern over the substrate. An exemplary material for masking layer 44 is photoresist. At least some of the photoresist 44 can remain within contact openings 42 as shown. Such remnant photoresist can serve to protect the device area. Although the trench patterns are illustrated as being generally wider in **dimension than the respective contact openings proximate which each is disposed, the patterns could have other dimensions,** e.g. narrower or the same width **dimensions as the contact openings**.

Claims Text CLTX 6 :
forming a layer of photoresist over the substrate and into the **contact opening onto the conductive portion of the line**;

Claims Text CLTX 7 :

patterning the photoresist to define a conductive **line pattern, at least some of the photoresist being received within the contact opening on the conductive portion of the conductive line** after the patterning; and

Claims Text CLTX 8 :
while photoresist is within the **contact opening on the conductive line** portion, selectively removing material of an uppermost of the first and second layers relative to the etch stop layer and defining a trough joined with the contact opening.

Claims Text CLTX 13 :
6. The semiconductor processing method of claim 1 further comprising removing the photoresist from over the conductive portion of the **line and thereafter filling the contact opening** with conductive material, the filling comprising: